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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,295	09/10/2003	Daisuke Yoshida	00684.002964.1	2456

5514 7590 07/06/2010

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
07/06/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,295	YOSHIDA, DAISUKE	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) *9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/505,194.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent ***Application No. 09/505,194*** (*now* ***Patent No. 6,670,938***), filed on ***16 February 2000***.

Drawings

2. The drawings were received on *20 April 2010*. These drawings are acceptable.

Specification

3. The amendment filed *29 September 2009* is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention.

The added material which is not supported by the original disclosure is as follows:

"At this time, the memory circuits 3, controlled by clock signals (MEMO_CLK), for memorizing respective offset correction data (e.g., of 5 bits) are reset to a prescribed level (e.g., 5 bit data of (10000) as a default)"

(*see line 5 of the replacement paragraph bridging pages 13 and 14*)

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. *Claims 8 and 11-15* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 8 recites the limitation "***a p-channel type***" (*line 22*). The addition of the word "***type***" to an otherwise definite expression extends the scope of the expression so as to render it indefinite. Ex parte Copenhaver, 109 USPQ 118 (Bd. App. 1955). It would be unclear to one having ordinary skill in the art what "***type***" is intended to convey. See MPEP 2173.05(b).

7. Claim 8 recites the limitation "***an n-channel type***" (*line 23*). The addition of the word "***type***" to an otherwise definite expression extends the scope of the expression so as to render it indefinite. Ex parte Copenhaver, 109 USPQ 118 (Bd. App. 1955). It would be unclear to one having ordinary skill in the art what "***type***" is intended to convey. See MPEP 2173.05(b).

8. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***the first supply voltage is set to be a voltage higher than the highest voltage by α and a voltage lower than the central voltage by α***" (*lines 11-12*).

It would be unclear to one having ordinary skill in the art how the "*first supply voltage*" can be set to both "*a voltage higher than the highest voltage*" and "*a voltage lower than the central voltage*."

Moreover, dependent claim 12 states, "*the α is in a range of 0 volt to 1 volt*" (*line 2*).

At α = 0 volts, the claim 11 subject matter: "***the first supply voltage is set to be a voltage higher than the highest voltage by [α = 0 volts] and a voltage lower than the central voltage by [α = 0 volts]***" makes no sense -- because the voltages are not actually higher or lower.

An omitted structural cooperative relationship results from the claimed subject matter: "***the second supply voltage is set to be a voltage higher than the central voltage by α and a voltage lower than the lowest voltage by α***" (*lines 12-14*).

It would be unclear to one having ordinary skill in the art how the "*second supply voltage*" can be set to both "*a voltage higher than the central voltage*" and "*a voltage lower than the lowest voltage*."

Moreover, dependent claim 12 states, "*the α is in a range of 0 volt to 1 volt*" (*line 2*).

At α = 0 volts, the claim 11 subject matter: "***the second supply voltage is set to be a voltage higher than the central voltage by [α = 0 volts] and a voltage lower than the lowest voltage by [α = 0 volts]***" makes no sense -- because the voltages are not actually higher or lower.

9. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

10. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. *Claims 8 and 11-14* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takahara et al (US 5,436,635 A)*** in view of ***Kubota et al (US 6,067,066 A)*** and ***the instant application's Admitted Prior Art (APA)***.

Regarding claim 8, ***Takahara*** discloses a liquid crystal apparatus [*e.g., Fig. 16*], comprising:

a liquid crystal device [*e.g., Fig. 11: T, P*]; and

a drive means [*e.g., Fig. 11: 11, 12*] for driving the liquid crystal device,

wherein the liquid crystal device comprises

an active matrix substrate [*e.g., Fig. 13: 31*] having thereon a plurality of signal lines [*e.g., Fig. 11: S*] arranged in columns,

a plurality of scanning lines [*e.g., Fig. 11: G*] arranged in rows,

pixel electrodes [*e.g., Fig. 11: P; Fig. 13: 33*] each connected via a pixel switch [*e.g., Fig. 11: T; Fig. 13: 34*] to an intersection of the signal lines and the scanning lines so as to supply positive [*e.g., Fig. 11: V+*] and negative [*e.g., Fig. 11: V-*] polarity picture signals to the pixel electrodes via the signal lines,

a counter substrate [*e.g., Fig. 13: 32*] disposed opposite to the active matrix substrate, and

a liquid crystal [*e.g., Fig. 13: 37*] disposed between the active matrix substrate and the counter substrate, and

wherein the drive means for driving the liquid crystal device includes:

a first common signal line [*e.g., Fig. 11: V(P)*] for supplying only the positive polarity picture signals to each of the plurality of signal lines,

a second common signal line [*e.g., Fig. 11: V(M)*] for supplying only the negative polarity picture signals to each of the plurality of signal lines,

a first transfer switch [*e.g., Fig. 11:* SW_{p1}] for connecting one signal line [*e.g., Fig. 11: S1*] with the first common signal line for selectively supplying only the positive polarity picture signals to the one signal line of the plurality of signal lines, and

a second transfer switch [*e.g., Fig. 11:* SW_{m1}] for connecting the one signal line with the second common signal line for selectively supplying only the negative polarity picture signals to the one signal line,

wherein the one signal line is connected to the first transfer switch and the second transfer switch,

~~wherein the first transfer switch comprises a first transistor of a p-channel type and the second transfer switch comprises a second transistor of an n-channel type; and~~

wherein the liquid crystal apparatus further comprises

an inversion drive means [*e.g., Fig. 11: a, 123, b*] for in a first frame, selectively turning on the first transfer switch for the one signal line, and

in a second frame, selectively turning on the second transfer switch for the one signal line

(*see the entire document, including Figs. 11 & 12; Column 12, Line 35 - Column 13, Line 17; Column 20, Line 24 - Column 21, Line 56*).

Takahara does not appear to expressly disclose the *first/second analog transfer switches comprising p/n-channel type transistors*, as instantly claimed.

However, ***Kubota*** discloses replacing analog switches [*e.g., Fig. 16: TO*] with a CMOS transfer switch [*e.g., Fig. 17: 21*] comprising an n-channel transistor [*e.g., Fig. 17: 21a*] and a p-channel transistor [*e.g., Fig. 17: 21b*]

(*see the entire document, including Column 22, Line 63 - Column 23, Line 16*).

Takahara and ***Kubota*** are analogous art, because they are both from the shared inventive field of driving liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to replace ***Takahara's*** transfer switches [*e.g., Fig. 11: SW*] with ***Kubota's*** CMOS transfer switches [*e.g., Fig. 17*], so as to lower conduction resistance (*e.g., see* ***Kubota****: Column 23, Lines 10-15*).

Should it be shown that ***Kubota*** discloses insufficient combinational motivation for ***Takahara's*** *first/second analog transfer switches comprising p/n-channel type transistors*, as instantly claimed:

The ***APA*** discloses, "*FIG. 18 is an equivalent circuit diagram for an active matrix-type liquid crystal device included in an active matrix-type liquid crystal display apparatus as an*

example of such a conventional liquid crystal apparatus. Referring to FIG. 18, the liquid crystal display apparatus includes a common signal line 701, vertical signal lines (data lines) 702-705, CMOS-type transfer switches 706-709, pixel switches 710, retention capacitors 711, a liquid crystal 712, a horizontal scanning circuit 713, a vertical scanning circuit 714, and scanning lines 715-718... Heretofore, CMOS-type switches have been used as the transfer switches 706-709. On the other hand, if an n-channel-type MOS (transistor) switch is used as the transfer switch, the switch-on resistance is increased as the picture signal voltage becomes higher due to a substrate bias effect, so that sufficient signal transfer becomes difficult. Reversely, if a p-channel-type MOS switch is used, the switch-on resistance is increased as the picture signal voltage becomes lower due to the substrate bias effect, so that sufficient signal transfer becomes difficult. For the above reason, a CMOS-type switch including both an n-channel and a p-channel has been used so as to attain a substantially constant on-resistance over an entire voltage range of picture signal" (*see the entire **APA**, including Pages 1-5 of the Specification*).

Takahara, ***Kubota***, and the ***APA*** are analogous art, because they are both from the shared inventive field of driving liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to replace ***Takahara's*** transfer switches [*e.g., Fig. 11: SW*] with the ***APA's*** CMOS transfer switches [*e.g., Fig. 18: 706-109*], so as to attain a substantially constant on-resistance over an entire voltage range of picture signal (*e.g., see the **APA**: Page 4*).

Regarding claim 11, ***Takahara*** discloses a picture signal-supplying means [*e.g., Fig. 3: 41, 42*] including

a first picture signal-generating means [*e.g., Fig. 3: 42; Fig. 4(a): +*] for generating the positive polarity picture signals supplied to the first common signal line and

a second picture signal-generating means [*e.g., Fig. 3: 42; Fig. 4(a): -*] for generating the negative polarity picture signals supplied to the second common signal line,

wherein the first picture signal-generating means generates the positive polarity picture signals in a range between a highest voltage [*e.g., Fig. 5: +Vm*] and a central voltage [*e.g., Fig. 5: Vo*] supplied to the pixel electrodes;

the second picture signal-generating means generates the negative polarity picture signals in a range between the central voltage and a lowest voltage [*e.g., Fig. 5: -Vm*] supplied to the pixel electrodes;

the first picture signal-generating means is operated at a first supply voltage [*e.g., Figs. 3-5: via selective V, GND, Vc summation = V(P) supplied to source drive IC 11*] and

the second picture signal-generating means is operated at a second supply voltage [*e.g., Figs. 3-5: via selective V, GND, Vd summation = V(M) supplied to source drive IC 12*] different from the first supply voltage;

the first supply voltage is set to be a voltage higher than the highest voltage by α [*e.g., wherein α = 0 volts*] and a voltage lower than the central voltage by α [*e.g., see Fig. 5: 61*]; and

the second supply voltage is set to be a voltage higher than the central voltage by α and a voltage lower than the lowest voltage by α [*e.g., see Fig. 5: 62*],

wherein the α denotes a voltage lowering margin due to an internal resistance [*e.g., Fig. 4(a): Ra, Rb*] in the first picture signal-generating means or in the second picture signal-generating means (*e.g., see Column 13, Line 20 - Column 16, Line 46*).

Regarding claim 12, ***Takahara*** discloses the α is in a range of 0 volt to 1 volt [*e.g., wherein α = 0 volts*] (*e.g., see Column 13, Line 20 - Column 16, Line 46*).

Regarding claim 13, ***Takahara*** discloses the first and second transfer switches and the picture signal-supplying means are disposed on the active matrix substrate (*e.g., see Column 13, Lines 20-35*).

Regarding claim 14, ***Takahara*** discloses the active matrix substrate comprises an insulating substrate (*e.g., see Column 12, Lines 63 - Column 13, Line 17*).

14. *Claim 15* is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Takahara et al (US 5,436,635 A)***, ***Kubota et al (US 6,067,066 A)***, and ***the instant application's Admitted Prior Art (APA)*** as applied to *claim 13* above, and further in view of ***Hoshi et al (US 5,691,794 A)***.

Regarding claim 15, ***Takahara***, ***Kubota***, and the ***APA*** do not appear to expressly disclose a *single crystal substrate*, as instantly claimed.

However, ***Hoshi*** discloses an active matrix substrate [*e.g., Figs. 2A-2D*] comprising a single crystal substrate [*e.g., Figs. 2A-2D: 9*]

(*see the entire document, including Column 2, Line 30 - Column 3, Line 33*).

Takahara, ***Kubota***, the ***APA***, and ***Hoshi*** are analogous art, because they are both from the shared inventive field of driving liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Hoshi's*** single crystal substrate [*e.g., Figs. 2A-2D: 9*] to form ***Takahara***, ***Kubota***, and the ***APA's*** combined active matrix substrate, so that extremely high quality display images can be obtained (*e.g., see the* ***Hoshi****: Column 3, Lines 7-11*).

Response to Arguments

15. Applicant's arguments filed on *20 April 2010* have been fully considered but they are not persuasive.

The Applicant contends, "*the phrase 'controlled by clock signals (MEMO_CLK)' is not new matter and is supported at least by Figs. 1 and 2 of the application filed on September 10, 2003. Both of these figures clearly show that memory circuit 3 is controlled by clock signals MEMO_CLK*" (see Page 9 of the Response filed on *20 April 2010*). However, the examiner respectfully disagrees.

Figures 1 and 2 nowhere state, indicate or imply that the illustrated "*MEMO_CLK*" (or "*MEMO-CLK*" for that matter) "*controls*" the memory circuits (3). The examiner respectfully notes a line has been illustrated in Figure 1 between the memory (3) and the adder (4). Is it the

Applicants position that the adder (4) must "*control*" the memory (3) simply because of the illustrated line between them? Does Figure 1's Analog-Out "*control*" the DAC (1)?

Applicant's arguments with respect to *claims 8 and 11-15* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

16. Applicant's amendment necessitated any new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
1 July 2010